A NEW PLANAR OUTPUT INDUCTOR FOR HIGH CURRENT, LOW VOLTAGE, DC-DC CONVERTERS

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ABSTRACT

A new, low profile, low loss, high power density output inductor, made utilizing high frequency low loss ferrite and an extremely low loss planar winding configuration for use in high current, low voltage DC-DC converters is presented. The key parameters of the output inductor that affect the total performance of the DC-DC Converter are characterized in this paper. The main point of this paper is to show the effect that the output inductor characteristics have on the total dc-dc performance. For example, the often-neglected "parasitic inductance" can cause unwanted loss of efficiency, and create conducted and radiated EMI due to the resonant circuit formed by the output capacitance of the switching MOSFET, synchronous MOSFET and the circuit inductance:

$$f := \frac{1}{2 \cdot \pi \cdot \sqrt{L_{stray} \cdot C_{oss}}} \qquad (1)$$

This paper will present ways of minimizing parasitic inductance via inductor construction techniques and positioning in the circuit layout. Finally, a new, low loss helical winding technique for the construction of low profile output chokes handling converter currents of 15 Amps to 200 Amps is introduced.

1. INTRODUCTION

To provide low voltage and high current to microprocessor and other logic circuits, there has been a lot of interest in the power industry in using parallel arrays, referred to as polyphase, multi-phase, slice or synchronized DC-DC converters operating at relatively high frequencies (500kHz to 750kHz). The advantage of these various parallel approaches is in lowering the total ac and dc resistance in these 1V, 100 Amp power sources. When this technique is implemented with low loss resonant switching, high efficiency, as well as, good dynamic response gains are possible. But there are an **optimum** number of parallel, interleaved converters in any specific application; the more current each circuit block can handle, the fewer blocks that will be needed. Since reliability is tied in with stress levels versus component count, the determination of the optimum number of parallel modules in the specific application is essential. In addition, many applications require low profile, planar components in order to meet the lower standard board height requirements. The limiting component in low profile applications is often the **output inductor**. In order to optimize the design, a wide choice of inductance values and MOSFET

building blocks must be available to the circuit designer. This paper will show the output inductor parameters effect on the converter performance.

The following effects will be analyzed:
1. Inductor DCR effect on converter performance
2. Inductor ACR effect on converter performance
3. Effect of stray inductance on efficiency and performance
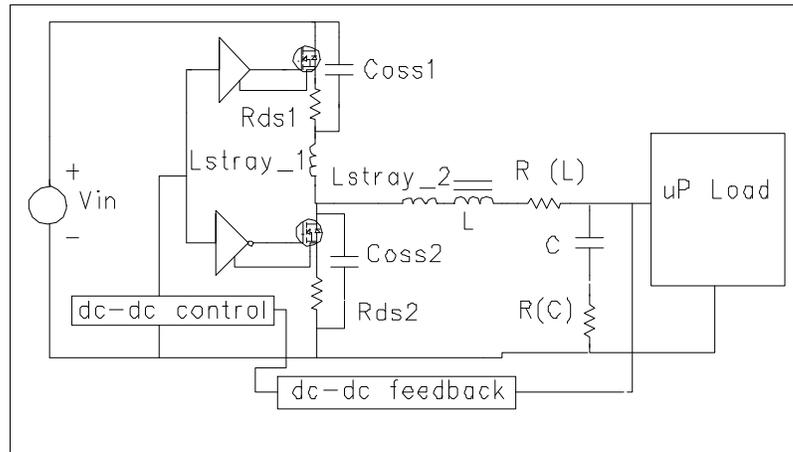

FIGURE 1

New requirements for the output inductor:

The next generation of microprocessors require the following parameters from the dc-dc converter providing the main voltage to the processor: 1) lower output impedance in order to meet the transient response requirements (the total converter impedance must be low enough to keep the voltage from sagging during a rapid change in load current demand). 2) Lower impedance through the inductor path in order to meet the requirements of dynamic voltage programming whereby the converter must respond to programmed output voltage changes [1]. Note that a large output capacitance value works against meeting this requirement in that it can trap excess charge at the time the voltage is programmed to be a lower value. The key parameter that must be managed is the total switched node impedance which as can be seen from Figure 1, is the inductor impedance, the upper and lower MOSFET impedance of the synchronous rectifier or the forward drop of the recovery diode. In many applications, optimization must be made between the **minimum inductance required for continuous mode operation** (low noise operation) and **maximum inductance allowed for transient response**. Fortunately, as the typical dc-dc converter frequency has gone up the inductance value required has gone down. But the designer still requires a wide range of inductors with a range of inductance and current values to optimize the design to the specific application. The microprocessor manufacturers have no intention of slowing the trend for ever higher and higher currents at ever lower and lower

voltages. By as early as 2010 the high performance IC will require 250 Amps at 0.5 Volts [2], which would likely be powered by as many as five 50 Amp converters.

2. Effect of inductor DCR on converter performance

One important source of loss in the converter is the output inductor DCR (dc winding resistance). This parameter defines the **minimal loss condition** of the inductor. By looking at just the simple DCR specified for the inductor, the circuit designer can get a quick idea of the impact on converter efficiency of the output inductor:

For example, if we let DCR = 1 milliOhm, where DCR = the inductor dc resistance,

And let I=100 Amps, where I = the converters DC output current,

Since P(inductor, dc loss) =

$$I^2 \cdot DCR \qquad (2)$$

$$= \quad 10 \text{ Watt}$$

If the converter was to provide 100 Amps at 0.75 Volts, the loss in efficiency due to the inductor DCR would be:

$$\eta_{loss}$$

$$=$$

$$\left[1 - \frac{V_{out} \cdot I_{out}}{\left(V_{out} \cdot I_{out} \right) + P_{d.inductor}} \right] \cdot 100\% \qquad (3)$$

$$= \quad 11.76 \text{ \% loss,}$$

This result demonstrates that the converter would be less than 89% efficient due to DCR alone. As can be seen from Figure 2, the impact of just 1 milliOhm of DCR becomes unacceptable in a 100 Amp or greater converter. Therefore a winding construction technique that minimizes DCR is a crucial requirement in the output inductor. Figure 3 shows a new winding construction technique that maximizes conductive copper cross section per turn, which is essential in lowering DCR. The helical wound coil provides the best way to get from layer to layer of inductive coil without incurring feed through loss. The rectangular coil cross section allows turns to be stacked very closely. Various high dielectric strength epoxy coil coatings of just a few mils. allows core window fill factors of 80% to be achieved, compared to 50% using older winding methods. This winding technique is capable of creating DCR's in the tenths of milliOhms needed for cost effective, high output current converters. This winding technique, also known as the quasi-planar winding, can be mass-produced with special automated equipment capable of rolling out many turns per second.

Minimal Loss Condition: effect of Inductors DCR on the converter efficiency:

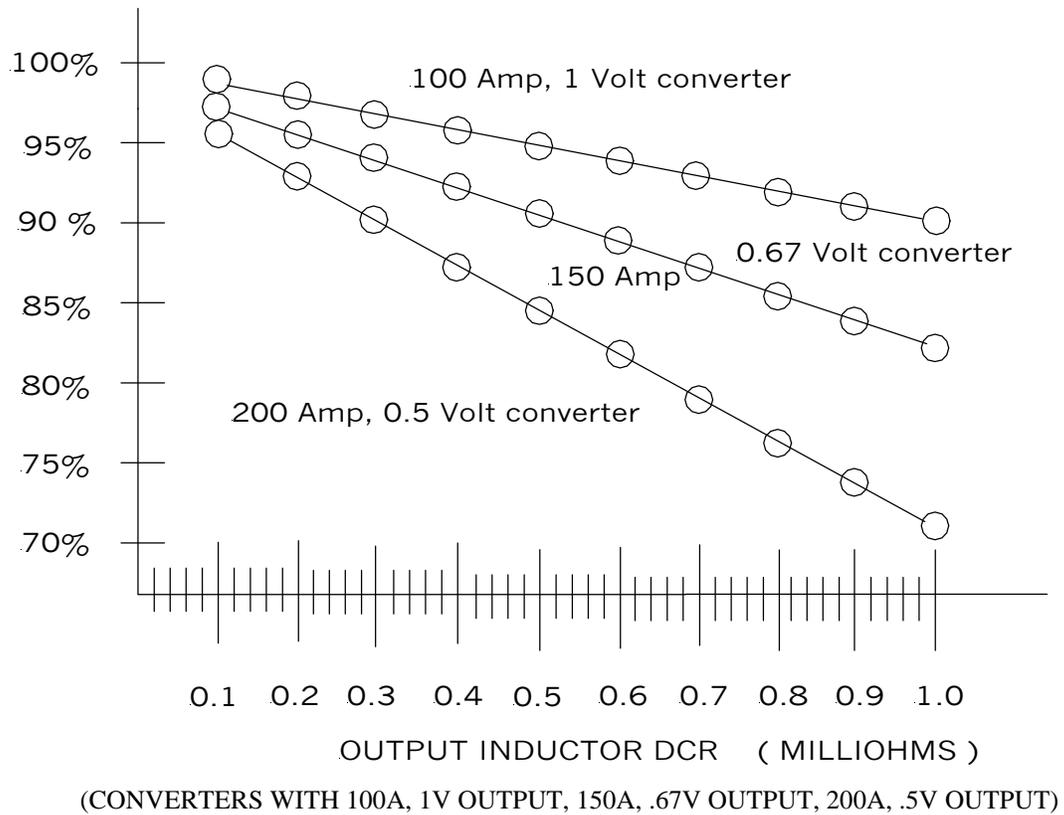## DROP IN EFFICIENCY AS A FUNCTION OF INDUCTOR DCR

100 Amp, 1 Volt converter

0.67 Volt converter

150 Amp

200 Amp, 0.5 Volt converter

100%
95%
90 %
85%
80%
75%
70%

0.1   0.2   0.3   0.4   0.5   0.6   0.7   0.8   0.9   1.0

OUTPUT INDUCTOR DCR   (MILLIOHMS)

(CONVERTERS WITH 100A, 1V OUTPUT, 150A, .67V OUTPUT, 200A, .5V OUTPUT)

Figure 2   Effect of inductor DCR on converter performance

Figure 3   QUASI-PLANAR WINDING TECHNIQUE

3. Inductor AC loss and its effect on converter performance

The ACR (ac winding resistance) is a function of the voltage, current, and frequency imposed on the inductor. The higher the inductor voltage, current and frequency are in the application, the more important the winding ac loss and core loss becomes. In the buck, non-isolated, down converter, the higher the input voltage bus is with respect to the output voltage, the greater the ac winding and core loss in the inductor.

Core loss:

As the volts per turn imposed on the output inductor increases, the higher the Eddy current loss in the **core** becomes in the application:

$$\text{Eddy current in the Core} \ \alpha \ \ \frac{d}{dt}\phi \ \ \alpha \ \ \left(\frac{\text{volts}}{\text{turn}}\right)^2 \quad\quad (4)$$

As can be seen from equation 4, the core loss goes up as the **square** of the volts per turn. In a 48 Volt input bus the core loss would be 4 times greater than in the comparable 24 Volt input bus.
Gapped ferrite usually outperforms powdered iron, and other lower resistivity (metal alloy) type cores at frequencies above 250kHertz. This is because ferrite has a relatively high resistivity, approximately 1.5 k Ohms – cm. as compared to metal alloy types that are in the tenths of milliOhms-cm. That is one reason why ferrite planar core structures such as the new low profile PQ and RM cores will continue to be good choices at these higher currents and frequencies.

AC winding loss:

Although core loss is relatively independent of frequency, ac winding loss is totally **dependent** on frequency. Two factors determine the ac winding loss: skin effect and proximity effect.
It has been shown [3][5] that the thinner and flatter the conductor used to make the inductor coil is, the lower the ac loss is at that particular frequency. The higher the frequency of operation the greater the ACR is compared to the DCR. The helical winding technique pictured in figure 3 can be adjusted in shape to achieve the optimum ACR to DCR balance at any given dc current versus ac current requirement. The greater the ripple current magnitude and frequency are in the application, the thinner the quasi-planar winding must be to keep the ac loss from exceeding the DCR loss. The following equations are useful in determining the optimum conductor thickness at the frequency of operation:

$$\text{D(pen)} \ = \ \frac{7.6}{\sqrt{f}} \quad \text{cm} \quad\quad (\text{copper}) \quad\quad\quad (5)$$

$$Rac \quad = \quad RDC \ \text{x} \ D(coil) \, / \, D(pen) \ \text{x} \ layers \qquad\qquad (6)$$

Where D(pen) is the skin depth of the operation frequency , and D(coil) is the coil thickness. This can be derived from Proxy [4] assuming a simple one layer planar inductor. Depending on the application, the amount of power lost to Rac, will be a function of the percent of ripple current to dc current. For example, if we have a 100 Amp, 1 Volt, 750 kHz, down converter, with a 6 % ripple content, the power loss due to Rac will be:

P(inductor, ac winding loss) =

$$i_{ripple}{}^{2} \ \text{x} \ R_{ac} \qquad\qquad (7)$$

= 2 Watts with a 1.27 mm thick planar coil
with a DCR of .45m Ohms, with a 3 turn coil

= 1.3 Watts with a 2.54 mm thick planar coil,
with a DCR of .15 m Ohms, with a 3 turn coil

Of course, Equation 6 applies only for flat helical windings where the magnetic field is uniform across most of the conductor's surface [4]. An output filter inductor typically has a smaller ac ripple current component and the optimum design has a much larger Rac/RDC ratio than planar transformers. Designing for low DCR is a priority in high current, low voltage output chokes.

4. Effect of stray inductance on efficiency and performance

Minimization of L-C oscillations in power circuits by lowering the stray inductance in the node between the switching MOSFET and the output inductor junction (fig.1) , and in the output inductor leads and construction (fig.4) will lower the emi and increase the efficiency of the converter. Although the circuit modeled in figure 4 is a synchronous buck , the equations that follow would also apply to a typical down converter with a schottky diode in place of the lower synchronous MOSFET. From classic time domain analysis it has been shown [6] that the oscillation that occurs when the upper fet turns off is governed by the value of the stray inductance in the circuit and the value of Coss which is nonlinear. If we assume in the models that the switches are ideal , but that they have parasitic, nonlinear capacitors across them , then equations 10 and 11 show the power loss as a function of Coss of the MOSFET and Lstray in the

circuit. An indication of the amount of EMI generated is shown by equations 9 and 10, which shows the duration of the oscillation after the upper MOSFET turns off.

$$C_{oss} \; \alpha \; \frac{1}{\sqrt{v_{ds}}} \qquad\qquad (8)$$

$$t_{oscillation} := \frac{2 \cdot C_{oss} \cdot \sqrt{v_{ds}}}{I_s} \qquad\qquad (9)$$

$$E_{loss} := \frac{1}{2} \cdot L_{stray} \cdot I_s^{\,2} \qquad\qquad (10)$$
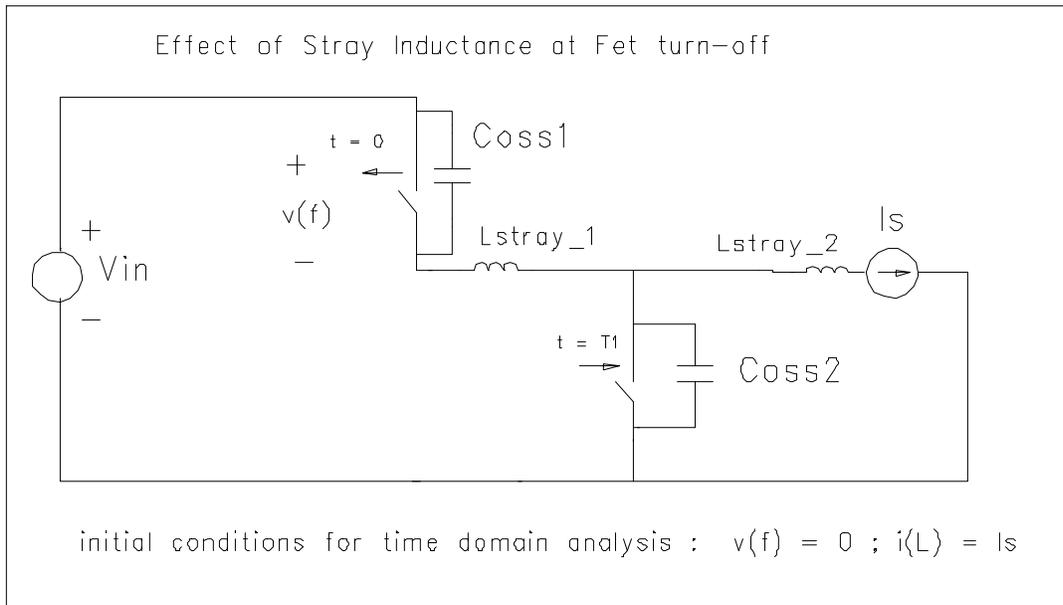
$$P_{loss} := E_{loss} \cdot f \qquad\qquad (11)$$

FIGURE 4

If we let Coss = 1000 pF, Vds = 48 V,   f = 750 kHz,   Is = 100 Amps, Lstray = 1.0 nH in a typical down converter modeled in figure 4 :

Then the oscillation time duration from equation 9 above would be .138 nanoseconds or in terms of frequency, 7.2 Ghz . We can see from equation 9 that the larger the MOSFET capacitance the larger the oscillation time.

From equations 10 and 11 we can calculate the power loss with these parameters to be :
P(loss) = 3.75 Watts. This example shows the effect that hard switching can have on the EMI generated in the circuit . If the distance between the 2 MOSFETS and the output inductor is increased ,
the power loss will go up as a function of the stray inductance . This parameter must be managed by proper positioning of the these components in the layout.

5. Managing Stray Fields in the Converter

Power loss is not the only problem that occurs with too much stray inductance. As the name implies , stray inductance is an inductance which is formed by stray fields not captured by the core of the magnetic element . Stray inductance is an inductance whose fields are in the surrounding air . Since this creates unwanted electromagnetic crosstalk in the adjacent circuits it is to be avoided if at all possible.

The output inductor itself must be of the enclosed core type , such as the various planar cores, pot cores, RM cores, and PQ cores . These cores shield the windings from the surrounding environment and therefore cut down on emission of stray fields. Some of the shapes to be avoided except at low power are toroids, which have exposed windings. Bobbin core designs are the worst offenders in that the flux path is completed through the air ! The hidden "half turn" found in many output inductors make the mistake of terminating on both sides of the inductor thus forcing the last turn to complete its flux path through the air.

Figure 5 and 6 show high current output inductors which have low emission of stray fields because the helical windings are almost entirely enclosed by the surrounding low profile PQ core . This shielding in addition to the small size which allows proper placement in the circuit layout, gives the converter designer a wide range of low noise output inductor solutions at high currents to choose from.
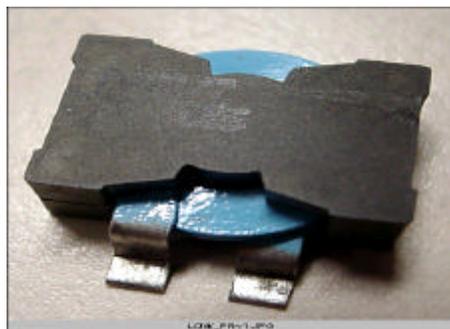

Figure 5   Example of helical winding enclosed in a PQ core that demonstrates the trade off between good shielding of the windings versus thermal radiation of heat from the windings. The unit pictured is a 1.4 uH, 1.2 mOhm, **30 Amp** output inductor.
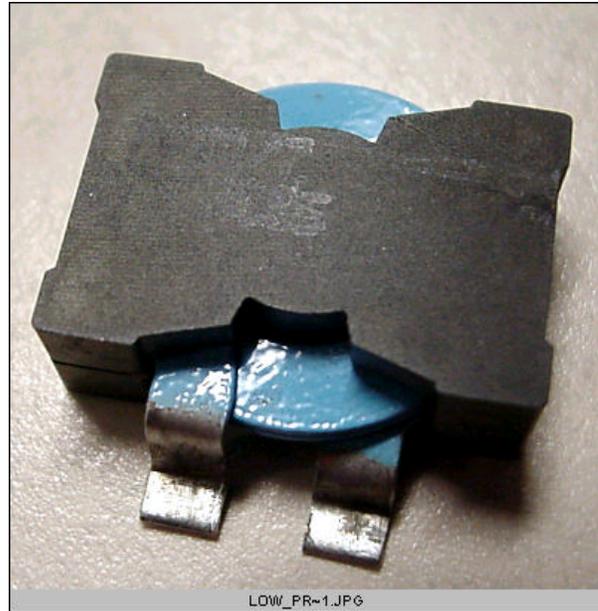
Figure 6. Typical Low profile inductor utilizing the new Quasi-planar winding construction technique to achieve low DCR, ACR, and low radiated emissions, at high inductor input voltages, currents, and frequencies. The output inductor pictured is a **70 Amp**, .9uH, .45 mOhm on a low profile PQ32 core.

6. Conclusion

The need for 25, 50,and 100 Amp output inductors for the dc-dc converters that will power the microprocessors of the future was discussed. The effect that the DCR, ACR, and the stray inductance of the output choke have on the converter performance was analyzed. A new construction method to use in creating the output inductor was discussed. And finally, the advantage that the flat helical winding has in minimizing loss via lower DCR, ACR, and stray inductance was shown. By adjusting the helical winding's thickness and width, a large variety of inductors can be produced when combined with the appropriate low profile core. The ability to meet the **minimum** inductance requirement for **continuous** mode dc-dc operation and still meet the efficiency and space requirements of the application has improved with these new output inductors. These new components will provide the power conversion specialist with a useful solution to his high current output inductor requirements well into the future.

7. Acknowledgements

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